

IN THE CLAIMS:

- 1 1. (Currently amended) A method of operating a cache coherency mechanism for a ~~dis-~~
2 ~~tributed~~ computer system that includes multiple processors, the method comprising
3 including the steps of:
 - 4 A. determining which processors have copies of data of interest;
 - 5 B. determining paths through various ~~system~~ switching devices on routes from an
6 associated home node to the processors that have copies of the data of interest;
 - 7 C. encoding information that is indicative of the paths into one or more masks;
 - 8 D. when the data of interest is the subject of an update operation, producing at the
9 home node an invalidate message that includes the masks;
 - 10 E. at one or more of the switching devices, decoding the applicable masks and
11 routing the invalidate message over the paths indicated by the decoded informa-
12 tion; and
 - 13 F. at the switching devices that connect to the processors, forwarding the invali-
14 date message to the processors that have copies of the data of interest.
- 1 2. (Currently amended) The method of claim 1, wherein the ~~step of~~ encoding includes
2 setting bits in a given mask to indicate paths from a corresponding switching device
3 to a next switching device on the routes to the processors.
- 1 3. (Currently amended) The method of claim 2, wherein the ~~step of~~ encoding further in-
2 cludes setting the bits to correspond to a combination of the paths through a plurality
3 of switching devices.
- 1 4. (Currently amended) The method of claim 2, wherein the ~~step of~~ encoding further in-
2 cludes setting bits that correspond to ports of the respective switching devices.

- 1 5. (Currently amended) The method of claim 1 wherein the encoding further includes
2 in the step of encoding
- 3 a. separately encoding into a first mask information relating to paths through
4 the switching device that is associated with the home node,
- 5 b. encoding into one or more second masks information relating to paths
6 through the switching devices that connect to the switching device of said sepa-
7 rately encoding into a first mask step-a,
- 8 e. encoding into one or more additional masks information relating to paths
9 through the switching devices that connect to the switching devices of said encod-
10 ing into one or more second masks the previous step, and
- 11 d. repeating said encoding into one or more additional masks step-e for paths
12 through additional switching devices.
- 1 6. (Currently amended) A method of operating a cache coherency mechanism for a ~~dis-~~
2 ~~tributed~~ computer system that includes multiple processors which are interconnected
3 by layers of switching devices, the method comprising ~~including the steps of:~~
- 4 A. determining which processors have copies of data of interest;
- 5 B. determining paths through various ~~system~~ switching devices on routes from a
6 home node to the processors that have copies of the data of interest;
- 7 C. encoding information that is indicative of the paths through a highest layer of
8 the system into a first mask;
- 9 D. encoding information that is indicative of the paths through a next highest
10 layer of the system into a next mask;
- 11 E. repeating said encoding information that is indicative of the paths through a
12 next highest layer step-D for the remaining layers of the system;
- 13 F. when the data of interest is the subject of an update operation, producing at the
14 home node an invalidate message that includes the masks;
- 15 G. at the switching devices in the highest layer, decoding the first mask and rout-
16 ing the invalidate message over the indicated paths;

17 ~~H.~~ at the switching devices in the remaining layers, decoding the corresponding
18 masks and routing the invalidate message over the indicated paths through the
19 layers; and
20 ~~I.~~ at switching devices that connect to the processors of interest, forwarding the
21 invalidate message to the processors.

1 7. (Currently amended) The method of claim 6, wherein the first and second steps of
2 encoding include setting bits in a given mask to indicate one or more paths from a
3 corresponding switching device to one or more switching devices in a next layer of
4 the system.

1 8. (Currently amended) The method of claim 6, wherein the first and second steps of
2 encoding further include setting the bits to correspond to a combination of the paths
3 through a plurality of switching devices in a given layer of the system.

1 9. (Currently amended) The method of claim 7, wherein the first and second steps of
2 encoding further include setting bits that correspond to ports of the switching devices.

1 10. (Original) The method of claim 6 wherein the highest layer includes one or more
2 switching devices that receive messages from the home node.

1 11. (Currently amended) A ~~distributed~~ computer system comprising including:
2 ~~A.~~ a plurality of processors, with one or more processors designated as home
3 nodes;
4 ~~B.~~ a plurality of switching devices that interconnect the processors;
5 ~~C.~~ one or more encoders for encoding into one or more masks information relat-
6 ing to paths through the switching devices from an associated home node to the
7 processors that have data of interest;
8 ~~D.~~ a cache coherency directory with entries for data of interest, the directory in-
9 cluding in a given entry

10 ~~a.~~ information that identifies the owner of the data, and
11 ~~b.~~ one or more associated masks; and
12 ~~E.~~ one or more decoders at the switching devices, the decoder in a given switch-
13 ing device decoding an associated mask to set paths through the switching device for
14 messages directed from the home node to processors that have copies of the associ-
15 ated data of interest.

1 12. (Currently amended) The ~~distributed~~ computer system of claim 11 wherein
2 ~~i.~~ the plurality of switching devices are organized into layers with one or more
3 switching devices in a highest layer connected to transmit messages from the home
4 node, one or more switching devices in a next highest layer connected to transmit
5 messages from the one or more switching devices in the highest layer to the switching
6 devices in a lower layer, one or more switching devices in lower layers connected to
7 transmit messages from the switching devices in preceding levels to switching de-
8 vices in subsequent layers, and one or more switching devices in a lowest level con-
9 nected to transmit messages to the processors, and
10 ~~ii.~~ the masks relate, respectively, to paths through the switching devices in the asso-
11 ciated layers.

1 13. (Currently amended) The ~~distributed~~ computer system of claim 12 wherein one or
2 more of the masks relate to combinations of the paths through the switching devices
3 in the associated layers.

1 14. (Currently amended) The ~~distributed~~ computer system of claim 11 wherein a given
2 home node produces messages directed to processors that have copies of data of in-
3 terest and includes in the messages the associated masks.

1 15. (Currently amended) The ~~distributed~~ computer system of claim 12 wherein the
2 switching devices are switches and the masks designate port of the associated
3 switches.

1 16. (Currently amended) The ~~distributed~~ computer system of claim 14 wherein the
2 switches that connect to the processors use local routing information to provide the
3 messages to the associated processors that have copies of the data of interest.

1 17. (Currently amended) The ~~distributed~~ computer system of claim 14 wherein the
2 switches that connect to the processors locally broadcast the messages to the associated
3 processors.